What is claimed is:

1. A semiconductor arrangement, in particular a diode, which takes the form of a chip (7) and has a first layer (2, 3, 4) of a first conductivity type and a second layer (20) of the opposite conductivity type; the first layer being made of at least two partial layers (2, 3), the first partial layer (2) having a first dopant concentration and the second partial layer (3) having a second dopant concentration, the second dopant concentration being less than the first, the second layer (20) being situated on the first partial layer (2), and the first partial layer (2) being situated on the second partial layer (3); wherein at least one trench (10) is introduced in the inner region (13) of the chip; the trench penetrating the first partial layer and extending to the second partial layer, and the trench being covered by a continuation region (23) of the second layer (20), so that at least one p-n junction is between the second layer (20) and the second partial layer (3), in the interior of the chip.

2. The semiconductor arrangement as recited in Claim 1, wherein the edge region (12) is beveled, so that further continuation regions (24) of the second layer, which are situated in the edge region, form additional p-n junctions together with the second partial layer.

3. The semiconductor arrangement as recited in Claim 1 or 2, wherein a third partial layer (4) is provided, which is connected to the second partial layer.

4. The semiconductor arrangement as recited in Claim 3, wherein a metallic coating (22) is provided, which is joined to the second layer, and an additional metallic coating (21) is provided, which is joined to the third

partial layer; and the concentrations of the second layer and the third partial layer are selected so as to ensure an ohmic contact between the second layer and the third partial layer, and the respective metallic coatings.

5. A method for manufacturing a semiconductor arrangement, where

in a first step, a semiconductor wafer (1) is provided, which includes a first layer (2, 3) having at least two partial layers, the first partial layer (2) being deposited on the second partial layer (3), the two partial layers being of a first conductivity type, the first partial layer having a first dopant concentration, the second partial layer having a second dopant concentration, and the second dopant concentration being less than the first;

in a further step, trenches (10) are introduced into the first layer, which extend through the first partial layer into the second partial layer;

in a further step, dopants of the opposite conductivity type are introduced into the topside of the wafer to change the conductivity type of a section of the first partial layer and a section of the second partial layer, in order to form a second layer (20); and

in a further step, metallic coatings (21, 22) are deposited on the topside and the bottom side of the wafer;

wherein, in a further step, the wafer is separated along the trenches, into individual chips, in such a manner, that each chip has at least one trench (10) in its

interior.

6. The method as recited in Claim 5, wherein the trenches are introduced by sawing them.

7. The method as recited in Claim 5, wherein the trenches are introduced by etching them.

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